--It is of pivotal importance for the present invention that the portion 105b of metal foil 105, which overlays the second opening 104, is mechanically shaped (preferably by bending or coining) into a position coplanar with the second surface 101b of the tape 101. Consequently, a metal foil offset 107 is formed around the periphery of opening 104. It is in this position that the portion 105a of metal foil 105 inside of opening 104 serves as mount pad for the integrated circuit chip 106. The foil portion 105a remains exposed after device 100 is encapsulated by encapsulation material 108, and is thus available for direct attachment to a printed circuit board 150, as shown in Figure 1B. This direct attachment, in turn, minimizes the thermal path, and thus optimizes the heat transport from chip 106 to the printed circuit board and to heat sink 160 as shown in Figure 1C.--

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Claims:

8. (twice amended) A low profile, high power semiconductor device including a plastic tape having first and second surfaces, comprising:

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a plurality of electrically conductive routing lines and a plurality of contact lands on said first surface, said lands exposed by first openings in said tape;

second openings in said tape configured to accommodate integrated circuit chips;

a chip mount pad covering each of said second openings, attached to said first surface and shaped to be coplanar with said second surface;

a circuit chip mounted by means of a thermally conductive material on each of said chip mount pads;

bonding wires connecting said chip to said contact lands;

encapsulating material surrounding said first tape surface including each of said mounted chips and said wire bonds; and

solder balls attached to each of said exposed lands.

18. (amended) A packaged integrated circuit, comprising:

a substrate having first and second opposing surfaces; said substrate including an opening extending through said substrate from said first surface to said second surface;

a chip mount pad comprising a sheet of metal, a portion of said sheet of metal on said first surface of said substrate and a portion of said sheet of metal covering said opening such that said portion of said sheet of metal covering said opening is coplanar with said second surface of said substrate, said portion of said sheet of metal covering said opening having first and second opposing surfaces, said second surface of said sheet of metal covering said opening being coplanar with said second surface of said substrate;

an integrated circuit chip mounted on said first surface of said sheet of metal in said opening.

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19. (amended) The packaged integrated circuit of Claim 18, further comprising encapsulant covering at least a portion of said first surface of said substrate and said chip, wherein said encapsulant does not cover said second surface of said substrate and does not cover said portion of said sheet of metal covering said opening that is coplanar with said second surface of said substrate.

20. (amended) The packaged integrated circuit of Claim 18, further comprising a heatsink attached to said second surface of said sheet of metal covering said opening.

21. (amended) The packaged integrated circuit of Claim 18, wherein said second surface of said sheet of metal covering said opening is attached to a printed circuit board.

22. (amended) A packaged integrated circuit chip, comprising:

a substrate having first and second opposing surfaces; said substrate including an opening extending through said substrate from said first surface to said second surface;

a chip mount pad of metal foil attached to said first surface of said substrate and downset into and covering said opening such that a bottom surface of said chip mount pad is coplanar with said second surface of said substrate;

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an integrated circuit chip mounted on a top surface of said chip mount pad;

encapsulation on said first surface of said substrate and not on said second surface of said substrate, such that said encapsulation covers said chip, but does not cover said bottom surface of said chip mount pad.

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25. (amended) A packaged integrated circuit chip, comprising:

a substrate having first and second opposing surfaces; said substrate including an opening extending through said substrate from said first surface to said second surface, said opening having a first size;

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a plurality of contact lands on said first surface of said substrate adjacent to said opening;

a chip mount pad of metal foil attached to said first surface of said substrate and downset into and covering said opening such that a bottom surface of said chip mount pad is coplanar with said second surface of said substrate;

an integrated circuit chip mounted on a top surface of said chip mount pad, said integrated circuit chip having a second size, wherein said second size is smaller than said first size;

bond wires coupling said integrated circuit chip to said contact lands; and

encapsulation on said first surface of said substrate and not on said second surface of said substrate, such that said encapsulation covers said chip, bond wires, and contact lands, but does not cover said bottom surface of said chip mount pad.
